IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
Kazuo NISHI et al.	)	ATTN: New Applications
Based On: JP 2003-002667	)	
Filed: January 8, 2003	)	
For: SEMICONDUCTOR DEVICE	)	
AND METHOD OF	)	
MANUFACTURING THEREOF	)	

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing references known to Applicant and requests that these references be made of record in the above identified application. Copies of the references listed are submitted herewith in accordance with 37 C.F.R. 1.98(a). Copies of U.S. patents and U.S. publications are not enclosed in accordance with the Notice published in the Official Gazette on August 5, 2003 entitled *Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003*, which waives the requirement under 37 CFR 1.98(a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. publication.

U.S. Patent Nos. 5,501,989; 5,589,694 and 5,744,822 are in the family of Japanese Patent Laid-Open No. 06-275808.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280. A duplicate copy of this sheet is attached.

Respectfully submitted,

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	1

Complete if Known	
Application Number	
Filing Date	January 2, 2004
First Named Inventor	Kazuo NISHI et al.
Group Art Unit	
Examiner Name	
Attorney Docket Number	0756-7243

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		5,501,989		Takayama et al.	03/26/1996	
		5,589,694		Takayama et al.	12/31/1996	
		5,744,822		Takayama et al.	04/28/1998	
		6,204,519		Yamazaki et al.	03/20/2001	
		6,198,133		Yamazaki et al.	03/06/2001	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP	06-275808			09/30/1994		Abst.

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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010085051 **Image available**
WPI Acc No: 1994-352764/199444
Related WPI Acc No: 1994-352761; 1994-352762; 1994-352763; 2001-106018; 2001-106199
XRAM Acc No: C94-160607
XRPX Acc No: N94-277001

Semiconductor circuit mfr. - by coating catalyst element on amorphous silicon@ film which promotes crystallisation with different density in active region of TFT and intrinsic region of thin film diode

Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Inventor: TAKAYAMA T; TAKEMURA Y
Number of Countries: 002 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6275808	A	19940930	JP 9386747	A	19930322	199444	B
US 5501989	A	19960326	US 94216107	A	19940321	199618	
US 5589694	A	19961231	US 94216107	A	19940321	199707	
			US 95411972	A	19950328		
US 5744822	A	19980428	US 94216107	A	19940321	199824	
			US 95483048	A	19950607		
			US 97788562	A	19970124		

Priority Applications (No Type Date): JP 9386747 A 19930322; JP 9386744 A 19930322; JP 9386745 A 19930322; JP 9386746 A 19930322
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6275808	A		8	H01L-027/146	
US 5501989	A		23	H01L-021/335	
US 5589694	A		23	H01L-029/78	Div ex application US 94216107 Div ex patent US 5501989
US 5744822	A		22	H01L-021/20	Div ex application US 94216107 Cont of application US 95483048 Div ex patent US 5501989

Abstract (Basic): JP 6275808 A

The manufacturing method semiconductor circuit forms a semiconductor film on a substrate (1) which consist of at least one TFD and TFT. The semiconductor film forms the active region of TFT as well as intrinsic region (17) of TFD. The semiconductor circuit is featured by the density of catalyser elements which promotes crystallisation in the active region of TFT and intrinsic region of TFD.

USE/ADVANTAGE - For use in image sensor. Processes substrate with large area at one stretch. Reduces manufacturing cost.

Dwg.1/4

Title Terms: SEMICONDUCTOR; CIRCUIT; MANUFACTURE; COATING; CATALYST; ELEMENT; AMORPHOUS; SILICON; FILM; PROMOTE; CRYSTAL; DENSITY; ACTIVE; REGION; TFT; INTRINSIC; REGION; THIN; FILM; DIODE

Derwent Class: L03; U11; U13; U14

International Patent Class (Main): H01L-021/20; H01L-021/335; H01L-027/146; H01L-029/78

International Patent Class (Additional): H01L-021/336; H01L-021/84; H01L-027/092; H01L-027/108; H01L-029/04; H01L-029/76; H01L-029/784

File Segment: CPI; EPI